Honors in VLSI Design

Department of Electronics and Communication Engineering

Table-III Honors in VLSI Design

S.No.	Semester	Course Code	Course Name	Category	Type	Credit	L-T-P
1	V		CAD ALGORITHMS FOR VLSI PHYSICAL DESIGN		Theory	3	3-0-0
2	V		CAD Algorithms for Synthesis of VLSI Systems		Theory	3	3-0-0
3	VI		Digital System Design & FPGA		Theory	3	3-0-0
4	VI		Formal Verification of Digital Hardware & Embedded Software		Theory	3	3-0-0
5	VII*		Micro-& Nano- electro-mechanical Systems (MEMS & NEMS)		Theory	3	3-0-0
6	VII*		Mixed Signal IC Design		Theory	3	3-0-0
7	VII*		Nanotechnology & Emerging Applications		Theory	3	3-0-0
8	VIII*		System Level Design & Modelling		Theory	3	3-0-0
9	VIII*		VLSI SIGNAL PROCESSING ARCHITECTURES		Theory	3	3-0-0
10	VIII*		VLSI Technology		Theory	3	3-0-0
11	VIII*		Quantum Computing		Theory	3	3-0-0
12	VIII*		Mini Project on VLSI Design		Practical	3	0-0-6

Course Name : CAD algorithms for VLSI physical design
Course Code :
Credits : 3 (L-T-P : 3-0-0)

Syllabus:

Unit 1: Introduction to CAD Algorithms Role of CAD in digital system design, levels of design, modelling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping

Unit 2: CAD Tools for synthesis CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as micro-programmes, PLAs, gate arrays etc. Technology mapping for FPGAs. Low power issues in high level synthesis and logic synthesis.

Unit 3: Architectural-Level Synthesis and Optimization Architectural Synthesis, Scheduling, Data path synthesis and control unit synthesis, scheduling algorithm, Resource Sharing and Binding

Unit 4: Logic-Level Synthesis and Optimization Two-Level Combinational Logic Optimization, Multiple-Level Combinational Logic Optimization, Sequential Logic Optimization

Unit 5: CAD Algorithms for VLSI Physical Design Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Ruleverification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis.

Course Outcomes :

CO1-Is able to grasp various operations on graphs, clique, coloring, partitioning etc

CO2-& apply graph algorithms and its applications into Boolean function representation (Knowledge)

CO3-Is able to grasp graph models for architecture representation (Knowledge)

CO4-Is able to analyse & implement two level/Multilevel/ sequential logic synthesis algorithms

CO5-(approximate & exact algorithms) (skills)

CO6-Is able to analyze & implement library binding algorithms- FSM equivalence & optimization (skills)

CO7. To able to grasp core concept of VLSI Physical Design. (Knowledge)

References:

1) G. D. Micheli. Synthesis and optimization of digital systems.
2) Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3) T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.
4) N. Deo, Graph Theory, PH India.
5) Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
6) Sherwani, N. VLSI physical design automation. Kluwer, 1999.

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Course Name : CAD ALGORITHMS FOR SYNTHESIS OF VLSI SYSTEMS
Course Code :
Credits : 3 (L-T-P : 3-0-0)

Syllabus:

Unit 1: **Introduction to CAD Algorithms**
Role of CAD in digital system design, levels of design, modeling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping

Unit 2: **CAD Tools for synthesis**
CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as microprogrammes, PLAs, gate arrays etc. Technology mapping for FPGAs. Low power issues in high level synthesis and logic synthesis.

Unit 3: **Architectural-Level Synthesis and Optimization**
Architectural Synthesis, Scheduling, Data path synthesis and control unit synthesis, scheduling algorithm, Resource Sharing and Binding

Unit 4: **Logic-Level Synthesis and Optimization**
Two-Level Combinational Logic Optimization, Multiple-Level Combinational Logic Optimization, Sequential Logic Optimization

Unit 5: **CAD Algorithms for VLSI Physical Design**
Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis

Course Outcomes :

CO1: Is able to grasp various operations on graphs, clique, coloring, partitioning etc & apply graph algorithms and its applications into Boolean function representation (Skills- Apply)
CO2: Is able to grasp graph models for architecture representation (Cognitive- understanding)
CO3: Is able to analyze & implement two level/Multilevel/ sequential logic synthesis algorithms (approximate & exact algorithms) (skills- Analyze)
CO4: Is able to analyze & implement library binding algorithms- FSM equivalence & optimization (skills- Evaluate)
CO5: To able to grasp core concept of VLSI Physical Design algorithms. (Cognitive- Apply)

References:

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.
4. N. Deo, Graph Theory, PH India.
5. Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
6. Sherwani, N. VLSI physical design automation. Kluwer, 1999.

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Course Name: Digital System Design & FPGA
Course Code :
Credits : 3 (L-T-P : 3-0-0)

SYLLABUS :

Sequential Logic Design- Introduction, Basic Bistable Memory Devices, additional bistable devices, reduced characteristics and excitation table for bistable devices.

Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Melay Machines,

Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs.

Data path and Control design.

Introduction to VHDL/Verilog- Data types, Concurrent statements, sequential statements, behavioral modeling.

Introduction to programmable logic devices- PALs, PLDs, CPLDs and FPGAs.

FPGA mapping of combinational & sequential designs

Books:

1. Digital System Design, Ercegovac, Wiley.
2. Richard S. Sandige, *Modern Digital Design,* McGraw-Hill, 1990.
3. Zvi Kohavi, Switching and Finite Automata Theory, Tata McGraw-Hill.
4. Navabi. Analysis and modeling of digital systems. McGraw Hill, 1998.
5. Perry. Modeling with VHDL. McGraw Hill, 1994.
6. Navabi. Verilog Digital Design. McGraw Hill, 2007.

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Course Name:Formal Verification of Digital Hardware & Embedded Software
Course Code :
Credits : 3 (L-T-P : 3-0-0)

SYLLABUS :

UNIT 1. Introduction to Design Verification, OVM and UVM methodology, case studies using Verilog and System Verilog, Static verification,

UNIT 2. Formal Verification of digital hardware systems- BDD based approaches, functional equivalence, finite state automata, FSM verification, Model checking, Various industry & academia CAD tools for formal verification.

UNIT 3. Verification, validation & testing - Debugging techniques for embedded software, instruction set simulators, clear box technique, black box testing, evaluating function test

UNIT 4. Recent trends in Design verification, case study

Course Outcomes:

CO1: To understand features of System Verilog (Cognitive- Understanding)

CO2: To study Assertion Based Verification and also be aware of functional coverage. (Cognitive- Analyze/Evaluate)

CO3: To apply language constructs of Bluespec for high level design/synthesis. (Skills- Apply)

CO4: To understand the necessity of the verification methodology. (Affective- understanding)

CO5: Ability to develop the test bench for DUT with verification methodology for scheduling, resource sharing and binding.(Skills- Creativity)

Additonal/optional Outcomes:

6) Understand significance of formal verification methodologies vis-à-vis simulation/ABV (Knowledge)

7) To perform equivalence check for combinational as well as sequential digital circuits (Thinking)

8) To develop Kripe structure based Model for sequential circuits and write PROPERTIES for Model Checking (Thinking)

9) To be able to use Model checking CAD tool- SMV or Cadence/Synopsys tool (SMV or Formality) (Skills)

Textbooks:

1. Discrete Structures, Logic and Computability- James L. Hein, Jones & Barlett India.
2. Logic- Schaum Series
3. [Chapter 2, Micheli, Synthesis of Digital Systems, McGrawHill]
4. Articles by Bryant, Eap, Akers on BDDs.
5. Advanced Formal Verification, R. Drechsler, Kluwer.
6. Algorithms & Data structures in VLSI Design, C. Meinel and T. Theobald, Springer.

References:

1. SystemVerilog IEEE standard;
2. BlueSpec user guide/standard;
3. Embedded systems Design- Artist Roadmap for Research & Development, LNCS-3436, Springer.
4. J. W. Valvano, Embedded microcomputer systems- Real Time Interfacing, , Thomson press (Cengage India)
5. Computers as components- Principles of embedded computing system design. Wolf, W., Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II, New Delhi-110 048.)
6. Verification, validation & testing in software engineering, A. Dasso and A. Funes, Idea Group Inc.
7. Hardware-Software codesign for data flow dominated embedded systems, R. Niemann, Springer.
8. Readings in Hardware/Software codesign, Micheli, Ernst, Wolf, Morgan Kaufmann.
9. Advanced Formal Verification, R. Drechsler, Kluwer.
10. Readings in Hardware/Software codesign, Micheli, Ernst, Wolf, Morgan Kaufmann.

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Course Name : Micro and Nano Electro Mechanical Systems
Course Code :
Credits : 3 (L-T-P : 3-0-0)

Syllabus:

Introduction to MEMS: Introduction: micro- and nano-scale size domains; scaling of physical laws; MEMS materials and processes; Miniaturization Issues. MEMS devices and applications, MEMS Market.

MEMS Fabrication Technology: Introduction to Submicron Technology: semiconductor materials; photolithography; doping; thin film growth and deposition; CVD, lithography and Ion Implantation, metallization; wet and dry etching; silicon micromachining; Bulk micromachining; Surface micromachining and LIGA.

MEMS Sensors and Actuators (Electrostatic, Thermal, piezoresistive): mechanics including elasticity, beam bending theory, membranes/plates; microactuators based on various principles, electrostatic, thermal, piezoresistive and applications e.g. acceleration, strain, tactile, temperature, IR detector flow; inkjet.

MEMS Sensors and Actuators (RF and Bio): MEMS Sensors and Actuators: mechanics including piezoelectric, magnetic, optical and its application. e.g. Microphone, micro speaker, nanogenerator, micro-motor, RF resonator, SAW filter. Materials and processes for BioMEMS, Applications.

MEMS Devices Packaging and Calibration: MEMS device Calibration and packaging techniques, Reliability. MEMS software training: COMSOL & Intellisuite.

Project The class project is to design reasonably complex MEMS devices. The project will be performed as a team of two or three students

Course Outcomes :

CO1- Gain a knowledge of basic approaches for various MEMS sensors and actuators design. (Cognitiveunderstaning)

CO2-Capability to critically analyze microsystems technology for technical feasibility as well as practicality. (Affective- Evaluate)

CO3 -Develop efficient design for improving device performance in terms of speed, sensitivity Selectivity and accuracy. (Skills- Create)

CO4- Design and optimization of RF MEMS sensors and actuators (Skills- Create)

CO5- Design and analysis of efficient MEMS presser sensor. (Skills- Analyze)

References:

1) Course notes – will be posted weekly on the course website
2) Foundations of MEMS, Chang Liu, Prentice Hall (2006)
3) Fundamentals of Micro fabrication, Marc Madou, CRC (2002)
4) Introduction to BioMEMS – Albert Folch, CRC (2012)

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Course Name : Mixed Signal IC Design
Course Code :
Credits : 3 (L-T-P : 3-0-0)

Syllabus:

Sample & Hold Circuits
Basic S/H circuits, effect of charge injection, compensating for charge injection, bias dependency, bias independent S/H

D/A Converter
General considerations, Static non-idealities & Dynamic non-idealities, Current steering DAC, Binary weighted DAC, Thermometer DAC, Design issues, Effect of mismatches

A/D Converter
General considerations, Static & Dynamic non-idealities, Flash ADC - Basic architecture, Design issues, Comparator & Latch, Effect of non-idealities, Interpolative and folding architectures, Successive approximation ADC, Pipeline ADC, Oversampling ADC - Noise shaping, Sigma-Delta modulator

PLLs
Basic Phase-Locked Loop Architecture, Voltage controlled oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Liberalized Small - Signal Analysis, Second - order PLL Model, Limitations of the second - order Small - Signal Model, PLL Design Example

References:
1. Behzad Razavi, "Principles of data conversion system design," S. Chand & Co. Ltd., 2000
2. Design of Analog CMOS Integrated Circuits: Behzad Razavi, Mc Graw Hill Education (India), 2018
3. VLSI Design techniques for Analog and digital Circuits: R. L. Geiger, P. E. Allen, D. R. Holberg, OUP, (2/E) McGrqw Hill (2002)
4. Jacob Baker, "CMOS Mixed-Signal Circuit design", A John Willy & Sons' inc' publications, 2003.
5. Analysis and Design of Analog ICs: Paul, Grey, et. al., J Willy and Sons, 4/E, 2001

Course Outcomes:
At the end of the course the student will be able to:
CO1: Understanding working of sample and hold circuits, compensation methods and bias independent design techniques.
CO2: Understanding basic of ADC, various design issues and their mitigation methods.
CO3: Understanding basic of DAC, various design issues and their mitigation methods.
CO4: Understanding the PLL principle of operation, working of its component, and the effects of the loop components on the system performance.
CO5: Design a phase-locked loop for application as a frequency synthesizer, frequency tracking filter, and demodulator for AM, FM.

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Course Name: Nanotechnology & Emerging Applications
Course Code :
Credits : 3 (L-T-P : 3-0-0)

SYLLABUS : Introduction: concept of nanotechnology, Origin of nanotechnology: change in optical, mechanical, electronic and magnetic behavior at nanoscale, Advantages of nanostructures in comparison to macrostructures, Scope of nanotechnology.

Categories of nanostructures and nanomaterials and their properties: Classification based on dimensionality: zero, one, two and three dimensional nanostructures:-Quantum Dots and Wells, nanowires, nanorods, nanoparticles, thin films, Carbon-based nano materials (buckyballs, nanotubes, graphene), Metallic nano materials (nanogold, nanosilver and metal oxides), Nanocomposites, Nanopolymers, Biological nanomaterials.

Synthesis of nanostructures and nanomaterials: Synthesis of nanoparticles, nanorods and nanowires, thin films: Ball Milling, Electrodeposition, Spray Pyrolysis, Flame Pyrolysis, Sol-Gel Processing, Solution Precipitation, Molecular Beam Epitaxy (MBE), Metal Nanocrystals by Reduction, Solvothermal Synthesis, Fundamental aspects of VLS and SLS growth, VLS growth of Nanowires, Control of the size of the nanowires, Template based synthesis, Chemical Vapor Deposition (CVD), Metal Oxide - Chemical Vapor Deposition (MOCVD), Physical vapor Deposition (PVD), Chemical vapour Deposition (CVD), DC/RF Magnetron Sputtering, Atomic layer Deposition (ALD).

Characterization of nanostructures and nanomaterials: Scanning Electron Microscopy (SEM), Field Emission Scanning Electron Microscopy (FESEM), High Resolution Transmission Electron Microscope (HRTEM), Scanning Tunneling Microscope (STM), Atomic Force Microscopy (AFM), X-ray Photoelectron Spectroscopy (XPS), Raman Spectroscopy, Infrared Spectroscopy, X-Ray Diffraction, Photoluminescence Spectroscopy, X-ray Fluorescence Method, Energy Dispersive Analysis of X-rays (EDAX), Thermogravimetry, Differential Thermal Analysis and Differential scanning calorimetry.

Applications: Application of nanotechnology in various domains: nano and molecular electronics, nano-devices like FinFETs, Tunnel-FETs, nanochemistry, nanobiotechnology, nanomedicine, nanomagnetism, nanorobotics, nanophotonics, smart nanosensors, MEMS/NEMS, nanotechnololgy for energy systems

References:

1. Nabok A., "Organic and Inorganic Nanostructures", Artech House, 2005.
2. Dupas C., Houdy P., Lahmani M., "Nanoscience: Nanotechnologies and Nanophysics", Springer-Verlag Berlin Heidelberg, 2007.
3. Edelstein A S and Cammarata R C, "Nanomaterials: synthesis, Properties and Applictions",Taylor and Francis, 2012.
4. Michael Wilson, Kamali Kannangara and Geoff Smith, "NANOTECHNOLOGY - Basic Science and Emerging Technologies", A CRC Press Company, D.C, 2002.;

Course Outcomes:
At the end of the course the student will be able to:
CO1: Knowledge of vast scope and capabilities of nanotechnology (Cognitive- understanding)
CO2: Acquaintance with various kinds of nanostructures and nanomaterials (Cognitive- Analyze)
CO3: Awareness of several kinds of synthesis and characterization techniques for nanostructures and nanomaterials (Cognitive- understanding)
CO4: Knowledge of applications of nanotechnology in various diverse domains.(Skills- Applying)

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Course Name : SYSTEM LEVEL DESIGN & MODELLING

Course Code :

Credits : 3 (L-T-P : 3-0-0)

Syllabus:

UNIT 1. Introduction: Embedded systems, electronic system-level (ESL) design, Models of Computation (MoCs): finite state machines (FSMs), dataflow, process networks, discrete event
UNIT 2. System-level design languages (SLDLs): SpecC, SystemC. System specification, profiling, analysis and estimation. System-level design: partitioning, scheduling, communication synthesis
UNIT 3. System-level modeling: processor and RTOS modeling, transaction-level modeling (TLM) for communication. System-level synthesis: design space exploration (DSE)
UNIT 4. Embedded hardware and software implementation: synthesis and co-simulation, case study. Application specific processors, Retargetable compilers, instruction set-simulation and co-simulation.
UNIT 5. System design examples and case studies. . Recent trends in system level design and modelling

Course Outcomes :

CO1- To model a problem at system level (Cognitive- Analyze)
CO2- Realize architecture for a design problem (Skills- Create)
CO3 -To model a system in System C language (Cognitive- Analyze)
CO4 -To generate system interface specifications and perform refinement (Skills- Create)
CO5- To appreciate HW-SW Co-design with latest trends (Cognitive- understanding)

References:

1) Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification,
2) Springer, September 2009. ISBN 978-1-4419-0503-1, ("Orange book", authors' site).
3) Gerstlauer, R. Doemer, J. Peng, D. Gajski, "System Design: A Practical Guide with SpecC",
4) Kluwer Academic Publishers, Boston, June 2001. ISBN 0-7923-7387-1 ("Yellow book")
5) T. Groetker, S. Liao, G. Martin, S. Swan, "System Design with SystemC", Kluwer Academic Publishers, Boston, May 2002. ISBN 1-4020-7072-1 ("Black book")
6) F. Vahid, T. Givargis, "Embedded System Design: A Unified Hardware/Software Introduction" (authors' site),
7) 7. John Wiley & Sons, 2001. ISBN 978-0-471-38678-0

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Course Name : VLSI Signal Processing Architectures
Course Code :
Credits : 3 (L-T-P : 3-0-0)

Syllabus:

Unit 1: Introduction to VLSI DSP Systems : Need of VLSI DSP algorithms. main DSP Blocks and typical DSP Algorithms. Fixed point /Floating point Representation; Floating point Arithmetic Implementation, Architectures of Adders/Multipliers; CORDIC, representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph.
Unit 2: Iteration Bound Data flow graph representations, loop bound and iteration bound, longest path matrix algorithm, iteration bound of Multirate data flow graphs.
Unit 3: Pipelining and Parallel Processing: Pipelining and parallel processing of FIR digital filters, pipeline interleaving in digital filters: signal and multichannel interleaving.
Unit 4: Retiming, Unfolding and Folding: retiming techniques; algorithm for unfolding, Folding transformation, Techniques of retiming, Unfolding & Folding.
Unit 5: Systolic Array Architecture Systolic Array Architecture: Methodology of systolic array architecture, FIR based Systolic Array, Selection of Scheduling Vector, Matrix multiplication of systolic array
Unit 6: Low power Design Theoretical background , Scaling v/s power consumption, power analysis, Power reduction techniques, Power estimation approach

Course Outcomes :

CO1-To understand Graphical representation of DSP algorithms and Mapping algorithms into Architectures (Cognitive/Skills- Apply)
CO2-To study architecture for real time systems and parallel and pipelining for Low power design (Cognitive- Remembering)
CO3-To be aware of systolic Array architecture and methodology for developing Architectures (Cognitive- Understanding)
CO4-To know different signal processing modules as convolution technique, retiming concept, folding /unfolding Transformation and CORDIC architecture. (Cognitive- Analyse)
CO5-To implement different low power Design techniques. (Skills- evaluate)

References:

1) VLSI Digital Signal Processing System : : Design and implementation by K.K. Parhi
2) Digital Signal Processing with Field Programmable Gate Arrays Uwe Meyer-Baese , Springer.
3) FPGA-based Implementation of Signal Processing Systems. by Roger Woods, John Mcallister, WILEY

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Course Name : VLSI Technology
Course Code :
Credits : 3 (L-T-P : 3-0-0)

Syllabus:

Crystal growth & wafer preparation: Processing considerations: Chemical cleaning, getting the thermal Stress factors etc.
Epitaxy: Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.
Oxidation: Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO2.
Diffusion: Diffusion –kinetics, Fick's law, sheet resistivity, methods of diffusion. Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.
Lithography: Optical Lithography optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-Ray, e-beam lithography.
Etching: Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching.
Thin Film Materials & their Deposition: Interlayer dielectrics in microelectronic devices, interconnections within and between different electronic devices. Packaging of Microelectronic Devices: Packaging materials, different types of packaging, Microelectronic devices reliability.

Course Outcomes :

CO1- An understanding of silicon and GaAs electronic device fabrication processes
CO2- Learn different types of operations involved in converting silicon wafer into a complex integrated circuit. Learn in detail basics of all operations used to manufacture a silicon-based monolithic integrate circuit.
CO3-Gain experience in the modelling and simulation of semiconductor manufacturing processes.
CO4-Develop an understanding of the working principle and operational details of semiconductor measurement device. DPGC Convener Head, ECE SPGB Chairman
CO5-Develop an understanding of industrially relevant and research intensive methods of electronic device fabrications. Students should develop understanding of silicon growth methods, thin film growth technologies, lithography and etching processes.
CO6-Become proficient in the measurements of key electrical parameters and characteristics of integrated circuits

References:

1) S. M. Sze, "VLSI Technology", McGraw Hill.
2) May, Sze, "Fundamentals of Semiconductor Fabrication", Wiley
3) Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, 1996.
4) Hong Xiao, "Introduction to Semiconductor Manufacturing", Prentice Hall, 2001.
5) SK Gandhi, "VLSI Fabrication Principles", John Wiley 1983.

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6) AB Glaser, GE Subak-Sharpe, "Integrated Circuit Engineering", Reading MA, Addison Wesley 1977.
7) D. Nagchoudhuri, "Principles of Microelectronic Technology", Wheeler Publishing, 1998.
8) Plummer, Deal , Griffin, "Slilcon VLSI Technology: Fundamentals, Practice and Modeling" , Pearson
9) Research papers published in Applied Physics Letters and IEEE journals

Course Name : Quantum Computing
Course Code :
Credits : 3 (L-T-P : 3-0-0)

Syllabus:

Introduction to Quantum Computing
Basics of quantum mechanics, quantum postulates, superposition, entanglement, No cloning theorem, Qubits, measurement on single and multiple qubits, Hilbert space, state vector Bra ket notation, Bloch sphere,

Quantum Computing and Networking Components
Single and two Qubit quantum gates, unitary transformation, composite state tensor product, cascade and parallel quantum circuits, Quantum diode, quantum router, quantum memory

Potential Quantum Algorithms
Quantum key distributions, quantum teleportation, Grover's algorithm (data base search) and Shor's algorithm (integer factorization), Deutsch–Jozsa algorithm, quantum Fourier transform (QFT), overview of open-source software for working with quantum computers at the level of circuits, and algorithms

Physical Realization of Quantum Circuits
Physical representation of Qubit, Nuclear magnetic resonance (NMR), Trapped ion, linear optics quantum computing (LOQC), Quantum electrodynamics (QED), Superconducting quantum computer

Application of Quantum Computing
Quantum communication and Cryptography, Quantum error correction (QEC), Quantum Machine learning, Big data search, Drug simulation

Course outcomes:
CO1: Understand basic concepts of quantum computing
CO2: Understand and analyze quantum switching, storage and computing devices
CO3: Apply and analyze quantum algorithms
CO4: Understand various quantum circuit implementation techniques
CO5: Design various applications of quantum computing
Reference Books:
1. Quantum Computation and Quantum Information" by Michael Nielsen and Isaac Chuang
2. Quantum computing : a gentle introduction / Eleanor Rieffel andWolfgang Polak.
3. Quantum Computing for Everyone" by Chris Bernhardt
4. Quantum Computing: An Applied Approach" by John Preskill
5. Quantum Computing: From Linear Algebra to Physical Realizations" by Masahiro Hotta and Keiji Matsumoto

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Course Name: Mini Project on VLSI Design

Course Code :
Credits : 3 (L-T-P : 0-0-6)

List of Experiments/ activities

Design, verification, prototyping and implementation of hardware.

Circuits and systems based on software, hardware, algorithms, concepts in emerging areas such as design of digital logic (combinational and sequencial circuit)on FPGA Boards, design of test bench using System C, System verilog for functional verification, modeling using TCAD and similar software, modeling and characterization of new devices/materials.

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